

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Docket No. A-64873-1/AJT/MSS

Anticipated Classification of  
this Application:

Class: 034 Subclass: 078

Prior Application: 09/018,021

Examiner: GRAVINI, S

Art Unit: 3744

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DATE OF DEPOSIT December 8, 1999

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TYPED NAME KARI BATEMAN

SIGNED

*Kari Bateman*

**Box PATENT APPLICATION FEE**

Assistant Commissioner for Patents  
Washington, DC 20231

Sir:

This is a request for filing a Divisional application under 37 C.F.R. 1.53(b), in the names of Jack Chihchieh Yao and Robert Jeffrey Bailey for WAFER CARRIER AND SEMICONDUCTOR APPARATUS FOR PROCESSING A SEMICONDUCTOR SUBSTRATE. This divisional claims priority to pending application Serial No. 09/018,021, filed on February 2, 1998.

1. ☒ Enclosed is a copy of the prior application.
2. ☒ Enclosed is a copy of the prior executed Declaration as originally filed.
3. (a) ☐ Enclosed is a Small Entity Affidavit.  
(b) ☐ A Small Entity Affidavit is of record in the prior application.
4. ☒ The filing fee is calculated below:

Claims as filed in the prior application, less any claims canceled by amendment below:

	(Col. 1)	(Col. 2)	SMALL ENTITY		OR	OTHER THAN A SMALL ENTITY	
FOR:	<u>NO. FILED</u>	<u>NO. EXTRA</u>	<u>RATE</u>	<u>FEE</u>		<u>RATE</u>	<u>FEE</u>
BASIC FEE				\$380	OR		\$760
TOTAL CLAIMS	<u>12</u> -20	= <u>0</u>	x 9 = \$	<u>  </u>	OR	x18 = \$	<u>  </u>
INDEP CLAIMS	<u>1</u> -3	= <u>0</u>	x39 = \$	<u>  </u>	OR	x78 = \$	<u>  </u>
[ ] MULTIPLE DEPENDENT CLAIM PRESENTED			+130 = \$	<u>  </u>	OR	+260 = \$	<u>  </u>
*If the difference in Col. 1 is less than zero, enter "0" in Col. 2.			TOTAL \$	<u>      </u>	OR	TOTAL \$	<u>760.00</u>

5. X The Commissioner is hereby authorized to charge any additional fees which may be required, including extension fees, or credit any overpayment to Deposit Account No. 06-1300 (Order No. A-64873-1/AJT/MSS).

6. X Our check in the amount of \$760.00 is enclosed.

7. X Cancel in this application original claims 13-23 of the prior application before calculating the filing fee. (At least one independent claim must be retained for filing purposes.)

8. X Amend the specification by inserting before the first line the sentence:

--This is a division of application Serial No. 09/018,021 filed February 2, 1998.--

9.    Formal drawings are enclosed.

10. (a)    Priority of application Serial No.        filed on        in        is claimed under 35 U.S.C. 119.

(b)    The certified copy has been filed in prior application Serial No.        filed on       .

11. X The prior application is assigned of record to Silicon Valley Group, Thermal Systems LLC.

12. X The power appears in the original papers in the prior application.

X Address all future communications to:

Maria S. Swiatek

FLEHR HOHBACH TEST ALBRITTON & HERBERT LLP

Suite 3400, Four Embarcadero Center

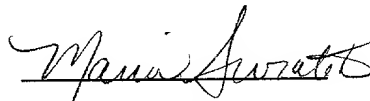
San Francisco, California 94111-4187

Telephone: (650) 494-8770

13.      A preliminary amendment is enclosed. (Claims added by this amendment have been properly numbered consecutively beginning with the number next following the highest numbered original claim in the prior application.)

14.   x   I hereby verify that the attached papers are a true duplicate of prior application Serial No. 09/018,021 as originally filed on February 2, 1998.

Date: December 8, 1999



Maria S. Swiatek, Reg. No. 37,244

Address of Signer:

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## WAFER CARRIER AND SEMICONDUCTOR APPARATUS FOR PROCESSING A SEMICONDUCTOR SUBSTRATE

5           The invention relates generally to the field of semiconductor processing and more specifically to a wafer carrier and semiconductor apparatus for processing a semiconductor substrate which minimizes contact with the backside of the substrate.

### BACKGROUND OF THE INVENTION

10           In the manufacture of semiconductors and integrated circuits, various films or layers of materials are deposited during the fabrication of such circuits. Dielectric films are widely deposited on semiconductor wafers to electrically isolate conductive layers and enable useful interconnects between such layers. Dielectrics, and other films, are often formed by chemical vapor deposition (CVD). The CVD process deposits a  
15           material on a surface of a substrate by transport and reaction of certain gaseous precursors on the surface. CVD reactors come in many forms. Low pressure CVD systems (LPCVD) and atmospheric pressure CVD systems (APCVD) operate on thermal CVD principles. Plasma may be employed to assist decomposition of chemicals for reaction in plasma enhanced CVD systems (PECVD), and in high density  
20           plasma (HDP) systems.

          Since CVD deposits the components of the precursor chemicals, it is important to minimize contaminants in the CVD reactor environment because such contaminants may become deposited in the film. Contaminants in the film damage the function of the devices on the wafer and reduce the device yields. Metal contamination is especially

detrimental on silicon wafers because the metal impurities can alter the properties of the wafer and devices after thermal processing and affect gate oxides.

Contaminants can arise from many sources. In addition to the presence of impurities in the precursor chemicals, contaminants can arise from the CVD systems themselves. During semiconductor processing metal atom contaminants may arise from some of the metal components making up the processing equipment. Such contaminants may be delivered to the semiconductor substrates where they contaminate the substrate surfaces and/or deposit in the film.

One source of metal contamination is the wafer support. In conventional systems, the wafer is typically in contact with the wafer support. During processing, contamination of the wafer can occur from the support. Additionally, contact with the wafer support can damage the backside surface of the wafer. This presents a problem when thin films are later deposited on the backside of the wafer. Scratches caused by contact with the wafer support can create defects in the films.

Moreover, for certain applications (called backseal applications) it is important that no deposition occur on the backside of the wafer during deposition on the front side of the wafer. Thus, not only is it important to minimize contact with the wafer for minimizing contamination and scratches on the wafer, it is at times important to seal the wafer from the deposition gases.

Prior art wafer carriers typically support the wafer by contacting a substantial area of the backside of the wafer. Such surface contact with the wafer promotes metal contamination and damaging of the backside surface. Another prior art wafer carrier, as described in U.S. Pat. No. 5,645,646, employs a plurality of support plates projecting from the surface of a plate to support the wafer. This design suffers from the same limitations, by providing surface contact with the wafer at a variety of locations. Moreover, this design allows deposition on the backside of the wafer and thus would not be suitable for backseal applications. It is desirable to provide a wafer support that minimizes surface contact with the substrate and is also capable of preventing deposition on the backside of the wafer.

## OBJECTS AND SUMMARY OF THE INVENTION

Accordingly, it is an object of the present invention to provide an improved wafer carrier.

More particularly, it is an object of the present invention to provide a wafer carrier that minimizes surface contact with a substrate thereby minimizing metal contamination and surface damage to the backside of a substrate.

It is a further object of the present invention to provide a wafer carrier that prevents deposition on the backside of a substrate.

A related object of the present invention is to provide a wafer carrier that promotes uniform deposition on the topside of a substrate.

These and other objects and advantages are achieved by the wafer carrier of the invention disclosed herein. The wafer carrier includes a circular plate having a flat edge region extending around the circumference of the plate. The plate has a circular recessed center region with a recessed bottom surface and includes an upwardly inclined surface around the periphery of the recessed bottom surface. A substrate (also referred to as a "wafer") is placed in the center region where it is supported by a portion of the upwardly inclined surface and is spaced apart from the recessed bottom surface such that the substrate is supported by the wafer carrier only around its peripheral edge.

## BRIEF DESCRIPTION OF THE DRAWINGS

Other objects and advantages of the present invention become apparent upon reading of the detailed description of the invention provided below and upon reference to the drawings in which:

FIG. 1 is a partial schematic view, partially in cross-section, of a chemical vapor deposition (CVD) system apparatus which may be employed with the present invention in accordance with one embodiment.

FIG. 2 is a top view of a wafer carrier in accordance with one embodiment of the present invention.

FIG. 3 is a cross-sectional side view of a portion of the wafer carrier in accordance with the present invention.

FIG. 4 is an enlarged cross-sectional side view of a portion of the wafer carrier showing placement of a wafer in accordance with the present invention

### DETAILED DESCRIPTION OF THE INVENTION

5           Turning to the drawings, wherein like components are designated by like reference numerals, FIG. 1 shows a schematic representation of an apparatus that can employ the wafer carrier of the present invention. FIG. 1 depicts a chemical vapor deposition (CVD) system 10 which generally includes a CVD reactor 20 and a gas delivery system 15 having conduits for delivery of gases to the reactor 20. CVD reactor 20 is shown as a conveyORIZED atmospheric pressure CVD (APCVD) type reactor, which is more fully described in U.S. Patent No. 4,834,020 and is herein incorporated by reference. It is important to note that although an APCVD reactor is shown, the inventive method may be practiced using other types of CVD reactors such as low pressure CVD (LPCVD), plasma enhanced CVD (PECVD) reactors, and high density plasma (HDP) reactors. The APCVD reactor 20 shown in FIG. 1 typically includes a muffle 31, a plurality of injectors 30 defining multiple stages (for simplicity only one injector 30, and thus one stage is shown) and a conveyor belt 34. The reactor 20 may comprise four stages, each of which are substantially identical. Within the muffle 31, a plurality of curtains 32 are placed around both sides of the injector 30 to isolate an area, and therebetween forming a deposition chamber area 33.

20           To deposit a film of material on the surface of a semiconductor device, a substrate 35 is placed on the conveyor belt 34 and is delivered into the muffle 31 and through the deposition chamber area 33. In the deposition chamber area 33, gaseous chemicals are conveyed by the injector 30 to the area proximate the surface of the substrate 35, wherein the gaseous chemicals react and deposit a film of material on the surface of the substrate 35.

25           In order to deposit layers of a desired composition and purity on the surface of the substrate 35, it is important that the wafer support secure the substrate without contaminating and/or damaging the surfaces of the substrate. The present invention promotes the reduction of contaminants and physical damage on the surface of the substrate by supporting the substrate at its peripheral edge. According to one

embodiment of the present invention, the substrate is placed in the wafer carrier and the wafer carrier is placed on the conveyor belt 34, which is then delivered to through the deposition chamber 33. In this particular example, a conveyORIZED type CVD reactor is shown. It should be understood, that a single wafer system where a single wafer is moved in and out of a single reactor chamber, may also be employed with the wafer carrier of the present invention.

The wafer carrier is shown in more detail with reference to FIGS. 2 and 3. The wafer carrier 40 comprises a circular plate 42 having a flat edge region 44 extending around the circumference of the plate 42, and a circular recessed center region 45. The recessed center region 45 comprises a recessed bottom surface 46 and an upwardly inclined surface 48 around the periphery of the recessed bottom surface 46. The edge region 49 of the recessed center 45 is perpendicular to the plane of the recessed bottom surface 46. Preferably, although it is not necessary, at least one opening 50 is provided in the bottom surface 46 of the circular recessed region 45. The opening receives a pin (not shown) which engages the wafer to receive and remove the wafer from the wafer carrier.

To support a substrate or wafer, the substrate is placed in the recessed center region 45 as shown in Fig. 4. Of particular advantage the wafer carrier of the present invention provides for supporting the wafer only around its peripheral edge. Specifically, the substrate is placed in the center region and is supported around its periphery by a portion of the upwardly inclined surface 48. The sole contact between the wafer and wafer carrier occurs on the inclined surface, where the curved surface of the wafer edge rests on the carrier. The rest of the wafer backside surface (that is the rest of the wafer besides its peripheral edge) is spaced apart from the bottom surface 46 and thus is not in contact with the wafer carrier. In an alternative embodiment, it is also possible that the inclined surface only extends along a radial distance sufficient to ensure contact with the wafer with a vertical step to the bottom of the carrier.

Preferably, the edge region 49 has a depth that is substantially the same as the thickness of the wafer "t" such that when the wafer is placed in the wafer carrier and contacts a portion of the upwardly inclined surface 48, the top surface of the wafer is substantially flush with the flat edge surface 44 of the wafer carrier. This enhances



deposition on the wafer by addressing what is known as the "edge effect." The edge effect is a phenomenon where the edge of the wafer creates disturbances in gas flow and/or temperature uniformity which reduce the uniformity of the deposited film. The edge effect is further minimized by the wafer carrier of the present invention, by effectively extending the edge of the wafer by the flat edge region 44. The edge effect now takes place over the flat edge region 44, leaving uniform deposition to occur along the entire surface of the wafer.

Of particular advantage, as shown in Fig. 4 the wafer contacts the wafer support only along the periphery of the wafer edge 50 where the wafer is supported by the inclined surface 48 of the recessed center 45. The point, or line contact, minimizes contact with the wafer in contrast to the surface contact made in the prior art carriers. By minimizing the surface contact, the present invention, the potential for surface damage and metal contamination is substantially reduced. Of further advantage, the present invention substantially eliminates the occurrence of deposition on the backside surface of the wafer. Since the wafer is supported around its entire periphery edge, the wafer is effectively sealed and deposition gases do not migrate to the backside of the wafer. This allows the processing of wafers in backseal applications. Again, this is in great contrast to prior art carriers which allow backside deposition to occur.

The wafer carrier can accommodate substrates of various sizes. Preferably, the wafer carrier will have a circular center region 45 with a diameter of approximately 200mm or 300mm, to accommodate a 200 or 300 mm wafer, respectively. However, the diameter of the center recessed region can be any size. The edge region 49 of the recessed center 45 will preferably coincide with the thickness of the wafer to be supported. For example, the edge region 49 will have a depth of approximately 0.75 to 0.80 mm for a 300mm wafer.

Preferably, to support the wafer the upwardly inclined surface 48 is inclined at an angle chosen to minimize contact with the surface of the backside of the wafer. The backside edge surface 50 of the wafer is curved with a roughly semicircular cross-section. The present invention provides for an inclined contact surface that contacts the wafer only on the curved wafer edge 50 and approaches line contact with the wafer around its perimeter. Preferably, the upwardly inclined surface 48 is inclined at an

angle in the range of approximately 5 to 45 degrees to the plane of the bottom recessed surface 46, with an angle of approximately 10 degrees being the most preferred.

To maintain the desirable line or point contact with the peripheral edge of the wafer and to provide secure support of the wafer, the thermal expansion of the wafer carrier is considered. Preferably, little thermal expansion occurs during the process so that the desired angle of the incline is preserved. Specifically, the wafer carrier is comprised of a material having a coefficient of thermal expansion in the range of  $2.6 \times 10^{-6}/^{\circ}\text{C}$  to  $5 \times 10^{-6}/^{\circ}\text{C}$ , with the lower values preferred. Materials with suitable coefficients of thermal expansion include silicon and silicon carbide.

Supporting the wafer by a portion of the upwardly tapered edge region 48 allows the wafer to be spaced apart from the bottom surface 46 of the circular center recessed region 45. The present invention provides for spacing the wafer from contact with the wafer carrier, thereby minimizing surface damage and metal contamination to the wafer, but while maintaining heat transfer to the wafer. To promote heat transfer to the wafer, the thermal conductivity of the wafer carrier is considered. Preferably, the thermal conductivity of the wafer carrier is in the range of approximately 40 to 70 W/m/K to promote good heat transfer. To meet both the coefficient of thermal expansion and thermal conductivity requirements, the wafer carrier is preferably made of a material selected from silicon carbide, aluminum nitride, large-grained polycrystalline silicon, and silicon/silicon carbide alloy.

The inventors have found that the spacing between the backside surface of the wafer and the bottom recessed surface 46 is important for a variety of reasons. First, the spacing's effect on heat transfer must be considered. Second, wafer deflection due to weight, temperature gradients and handling must be evaluated. These criteria are met with the present invention by providing a spacing between the backside surface of the wafer and the bottom recessed surface 46 that is in the range of approximately 0.15 to 0.5 mm, with a spacing of 0.25 mm being the most preferred for 300 mm wafers.

Thus, an improved wafer carrier has been provided. The wafer carrier minimizes metal contamination and damage to the substrate and is suitable for backseal applications. Experiments run with the wafer carrier of the present invention

demonstrate that the metal contamination in the films deposited on the wafer is reduced to nondetectable levels ( $< 10^9$  atoms/cm<sup>2</sup>).

- 5 The foregoing description of specific embodiments of the invention have been presented for the purpose of illustration and description. They are not intended to be exhaustive or to limit the invention to the precise forms disclosed, and obviously many modifications, embodiments, and variations are possible in light of the above teaching. It is intended that the scope of the invention be defined by the claims appended hereto and their equivalents.

## CLAIMS

What is Claimed:

1. A wafer carrier for supporting a substrate, comprising:  
a circular plate having a flat edge region extending around the  
circumference of said plate; and  
a circular recessed center region having a recessed bottom surface and including  
an upwardly inclined surface around the periphery of said recessed bottom surface,  
wherein the substrate is supported by a portion of the upwardly inclined surface  
and is spaced apart from said recessed bottom surface such that the substrate is  
supported by said wafer carrier only around the periphery of the substrate.
2. The wafer carrier of Claim 1 wherein said recessed bottom surface  
further comprises at least one aperture formed therein for receiving at least one support  
member to engage the substrate.
3. The wafer carrier of Claim 1 wherein said circular recessed center region  
has a diameter of approximately 200 mm.
4. The wafer carrier of Claim 1 wherein said circular recessed center region  
has a diameter of approximately 300 mm.
5. The wafer carrier of Claim 1 wherein said upwardly inclined surface is  
inclined at an angle in the range of approximately 5 to 45 degrees to the plane of the  
recessed bottom surface.
6. The wafer carrier of Claim 1 wherein said upwardly inclined surface is  
inclined at an angle of approximately  $10^\circ$  to the plane of the bottom recessed surface.
7. The wafer carrier of Claim 1 wherein said wafer carrier is comprised of  
a material having coefficient of thermal expansion in the range of  $2.6 \times 10^{-6}$  to  
 $5 \times 10^{-6}/^\circ\text{C}$ .

8. The wafer carrier of Claim 1 wherein said wafer carrier is comprised of a material having thermal conductivity in the range of 40 to 70 W/m/K.

5 9. The wafer carrier of Claim 1 wherein said wafer carrier is comprised of a material selected from the group of silicon carbide, aluminum nitride, large-grained polycrystalline silicon and silicon/silicon carbide alloy.

10 10. The wafer carrier of Claim 1 wherein the wafer is spaced apart from said recessed bottom surface by a distance of approximately 0.15 to 0.5 mm.

11. The wafer carrier of Claim 1 wherein the wafer is spaced apart from said recessed bottom surface by a distance of approximately 0.25 mm.

15 12. The wafer carrier of Claim 1 wherein said flat edge region has a width of approximately 5 to 25 mm.

16 13. A reactor for depositing a layer of material on a substrate, comprising:  
a deposition chamber;  
a wafer carrier in the deposition chamber, the wafer carrier having a circular plate  
20 with a flat edge region extending around the circumference of said plate, and a circular recessed center region having a recessed bottom surface and an upwardly inclined surface around the periphery of said recessed bottom surface, wherein the substrate is supported by a portion of the upwardly inclined surface and is spaced apart from said recessed bottom surface such that the substrate is supported by said wafer carrier only  
25 around the peripheral edge of the substrate;  
a gas inlet into the deposition chamber for conveying gases to the chamber; and  
an exhaust system for removing gases from the chamber.

30 14. The method of Claim 13 wherein said reactor is a low pressure CVD reactor.

15. The method of Claim 13 wherein said reactor is a atmospheric pressure CVD reactor.

5 16. The method of Claim 13 wherein said reactor is a plasma enhanced CVD reactor.

17. A CVD processing apparatus for processing a substrate, comprising:  
a muffle;  
at least one CVD chamber area within said muffle;  
10 at least one injector for conveying gases into said at least one CVD chamber area;  
a conveyORIZED belt passing through said chamber area and said muffle; and  
at least one wafer carrier placed on said conveyORIZED belt for moving the substrate  
though said chamber area whereby the gases process a surface of the substrate.

15 18. The CVD processing apparatus of Claim 17 wherein said wafer carrier further comprises:

a circular plate having a flat edge region extending around the circumference of said plate; and

20 a circular recessed center region having a recessed bottom surface and including an upwardly inclined surface around the periphery of said recessed bottom surface,

wherein the substrate is supported by a portion of the upwardly inclined surface and is spaced apart from said recessed bottom surface such that the substrate is supported by said wafer carrier only around the peripheral edge of the substrate.

25 19. The wafer carrier of Claim 18 wherein said upwardly inclined surface is inclined at an angle of approximately  $10^\circ$  to the plane of the recessed bottom surface.

30 20. The wafer carrier of Claim 17 wherein said wafer carrier is comprised of a material having coefficient of thermal expansion in the range of  $2.6 \times 10^{-6}$  to  $5 \times 10^{-6}/^\circ\text{C}$ .

21. The wafer carrier of Claim 17 wherein said wafer carrier is comprised of a material having thermal conductivity in the range of 40 to 70 W/m/K.

22. The wafer carrier of Claim 17 wherein said wafer carrier is comprised  
5 of a material selected from the group of silicon carbide, aluminum nitride, large-grained polycrystalline silicon and silicon/silicon carbide alloy.

23. The wafer carrier of Claim 17 wherein the wafer is spaced apart from said recessed bottom surface by a distance of approximately 0.15 to 0.5 mm.

## ABSTRACT

A wafer carrier is provided comprised of a circular plate having a flat edge region extending around the circumference of the plate. The plate has a circular recessed center region with a recessed bottom surface and includes an upwardly inclined surface around the periphery of the recessed bottom surface. A substrate is placed in the center region where it is supported by a portion of the upwardly inclined surface and is spaced apart from the recessed bottom surface such that the substrate is supported only around its edge. The wafer carrier minimizes surface contact with the substrate thereby minimizing metal contamination and surface damage to the backside of a substrate and prevents deposition on the backside of the substrate.



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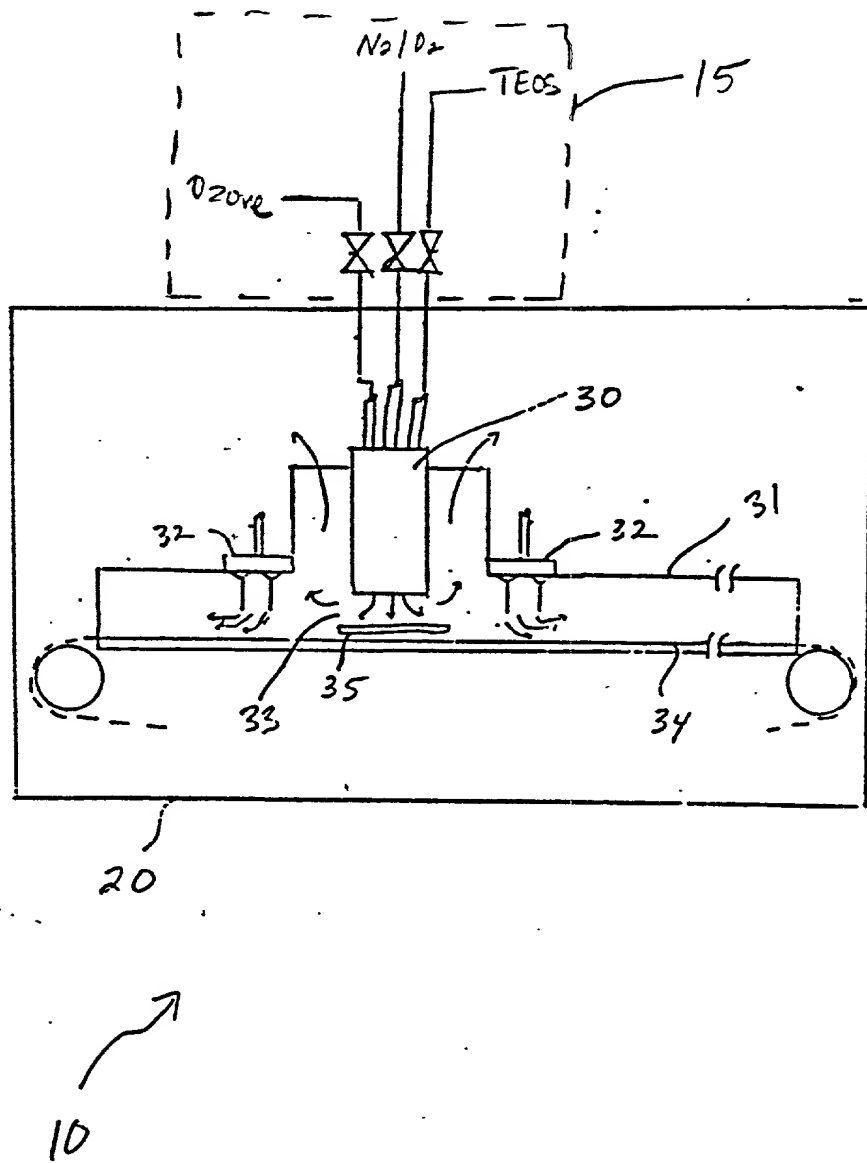


FIG 1

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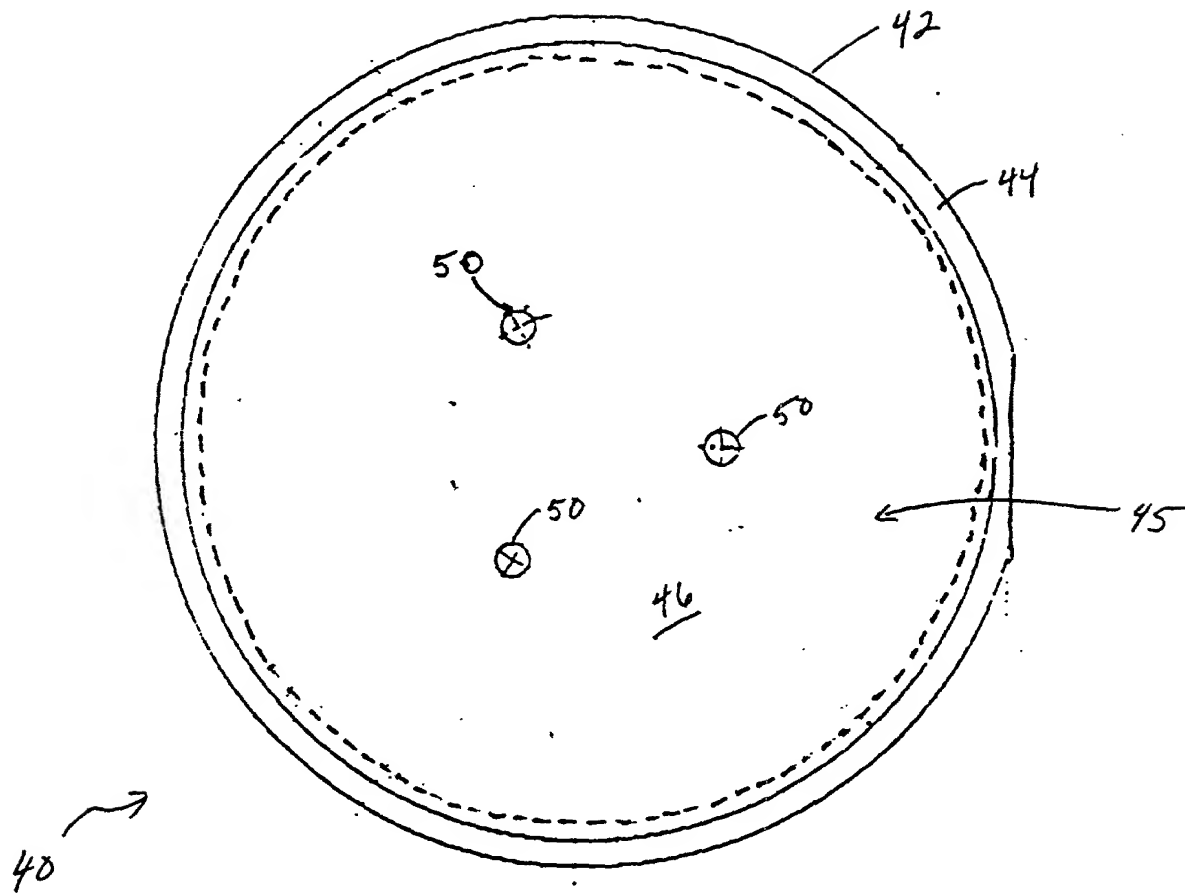


FIG-2

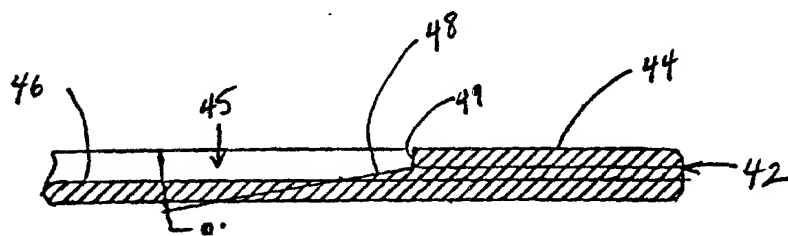
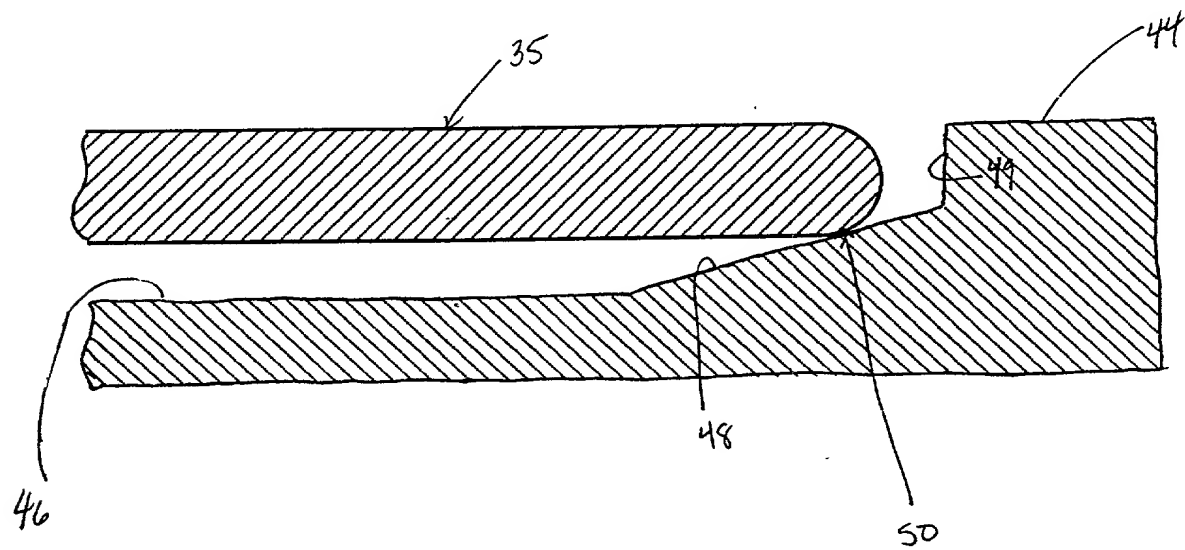


FIG-3



FIG\_4

## DECLARATION FOR PATENT APPLICATION

As a below-named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name ,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled **WAFER CARRIER AND SEMICONDUCTOR APPARATUS FOR PROCESSING A SEMICONDUCTOR SUBSTRATE**, the specification of which

☒ is attached hereto.

☐ was filed on \_\_\_\_\_ as  
Application Serial No. \_\_\_\_\_  
and was amended on \_\_\_\_\_ (if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the Patent Office all information known to me to be material to patentability as defined in 37 C.F.R. 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)

Priority Claimed

\_\_\_\_\_  
(Number)

\_\_\_\_\_  
(Country)

\_\_\_\_\_  
(Date Filed)

Yes ☐ No ☐

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose to the Patent Office all information known to me to be material to patentability as defined in 37 C.F.R. 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

\_\_\_\_\_  
(Application Serial No.)

\_\_\_\_\_  
(Filing Date)

\_\_\_\_\_  
(Status)  
(patented, pending, abandoned)

\_\_\_\_\_  
(Application Serial No.)

\_\_\_\_\_  
(Filing Date)

\_\_\_\_\_  
(Status)  
(patented, pending, abandoned)

Direct all telephone calls to Maria S. Swiatek at (650) 494-8700.

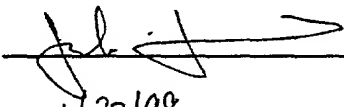
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San Francisco, California 94111-4187

File No. A-64873/AJT/MSS

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Title 18, United States Code, §1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole or  
first inventor: Jack Chihchieh Yao

Inventor's signature: 

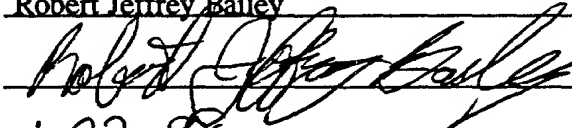
Date: 1/22/98

Residence: Scotts Valley, California

Citizenship: U.S.A.

Post Office Address: 118 A Christal Oaks Drive  
Scotts Valley, California 95066

Full name of second joint  
inventor, if any: Robert Jeffrey Bailey

Inventor's signature: 

Date: 1-22-98

Residence: Santa Cruz, California

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